L Number	Hits	Search Text	DB	Time stamp
1	90	SAC and plug	EPO; JPO; DERWENT; IBM_TDB	2004/08/12 09:14
2	58	438/229,299,303,586,587,597.ccls. and SAC and plug	USPAT; US-PGPUB	2004/08/12 09:15
3	225	438/229,299,303,586,587,597.ccls. and (SAC or aligned) and plug	USPAT; US-PGPUB	2004/08/12 09:20
4	181	(438/229,299,303,586,587,597.ccls. and (SAC or aligned) and plug) and @ad<20010813	USPAT; US-PGPUB	2004/08/12 09:20
5	334	257/202,211,296,311,316.ccls. and (SAC or aligned) and plug	USPAT; US-PGPUB	2004/08/12 09:20
6	221	(257/202,211,296,311,316.ccls. and (SAC or aligned) and plug) and @ad<20010813	USPAT; US-PGPUB	2004/08/12 09:20
7	218	((257/202,211,296,311,316.ccls. and (SAC or aligned) and plug) and @ad<20010813) not ((438/229,299,303,586,587,597.ccls. and (SAC or aligned) and plug) and @ad<20010813)	USPAT; US-PGPUB	2004/08/12 09:21

DERWENT-ACC-NO: 2003-873630

DERWENT-WEEK: 200381

TITLE: Method for manufacturing a semiconductor device is capable of reducing parasitic capacitance between an interconnection and a contact **plug**

INVENTOR: YOON, G H

PATENT-ASSIGNEE: HYNIX SEMICONDUCTOR INC[HYNIN]

PRIORITY-DATA: 2001KR-0088306 (December 29, 2001) BAD DATE

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2003059445 A	July 10, 2003	001		H01L 021/28

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2003059445A	N/A	2001KR-0088306	December 29, 2001

INT-CL (IPC): H01L021/28

ABSTRACTED-PUB-NO: KR2003059445A

BASIC-ABSTRACT:

NOVELTY - Method for manufacturing a semiconductor device is capable of reducing parasitic capacitance between an interconnection and a contact **plug**.

DETAILED DESCRIPTION - Interconnections (20A) and a hard mask (30) are sequentially stacked on a semiconductor substrate (10). The width of the

interconnection (20A) is reduced by under-cutting of the interconnection. An
interlayer dielectric (40) is formed to fill the under-cut portion. A contact
hole is formed by etching the interlayer dielectric (40) by using self aligned
contact (**SAC**) processing. A contact **plug** (80) is formed by filling a
conductive layer into the contact hole. At this time, the interlayer
dielectric (40) remains at both sidewalls of the interconnection.

CHOSEN-DRAWING: Dwg.1/10

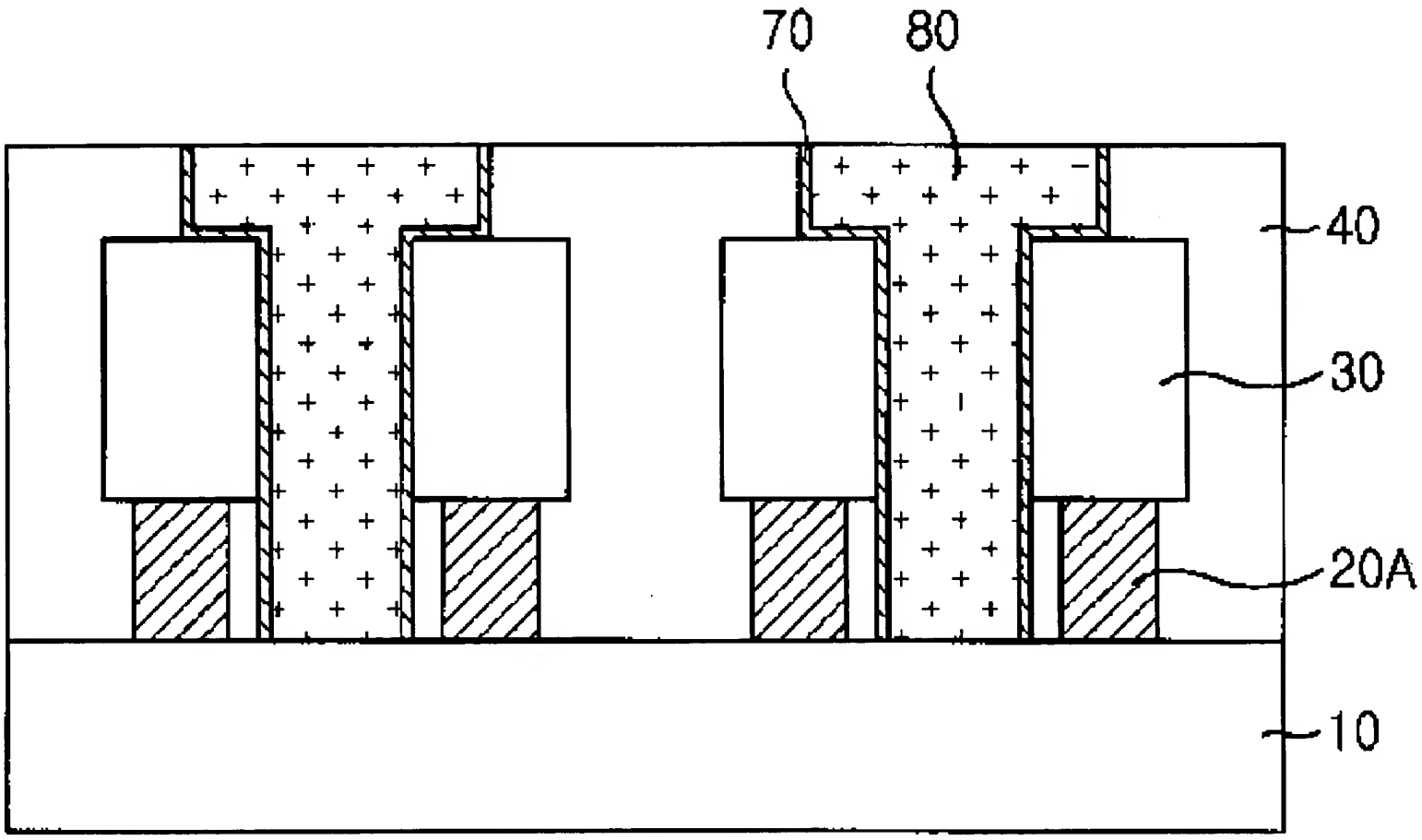
TITLE-TERMS: METHOD MANUFACTURE SEMICONDUCTOR DEVICE CAPABLE REDUCE PARASITIC
CAPACITANCE INTERCONNECT CONTACT **PLUG**

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C07; L04-C12; L04-C13A; L04-C13B;

EPI-CODES: U11-C05B9B; U11-C05D1; U11-C05D3; U11-C05D4; U11-C05E3; U11-C05F1;
U11-C05G2C;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C2003-246607


70
80
40
30
20A
10